AT91SAM7L-STK Rev. A Starter Kit

User Guide

6409A–ATARM–30-Jun-08

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Section 1

Overview

1.1 Scope

The AT91SAM7L-STK rev.A starter kit enables evaluation capabilities and code development of applications running on an AT91SAM7L64/128.

This guide focuses on the AT91SAM7L-STK rev.A board as an evaluation platform.

1.2 Deliverables

The AT91SAM7L-STK rev.A package contains the following items:

- An AT91SAM7L-STK rev.A board
- Two AAA batteries

1.3 The AT91SAM7L-STK Rev. A Starter Board

The board is equipped with an AT91SAM7L128 (128-lead LQFP package) together with the following:

- One DBGU serial communication port
- One ZIGBEE extension connector
- One JTAG/ICE debug interface
- Five user- input push buttons
- One WakeUP input push button
- One Reset Push Button
- One Battery Socket for two AAA batteries
- One 400 segments dot matrix LCD

Section 2

Setting Up the AT91SAM7L-STK Rev. A Board

2.1 Electrostatic Warning

The AT91SAM7L-STK rev.A starter board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

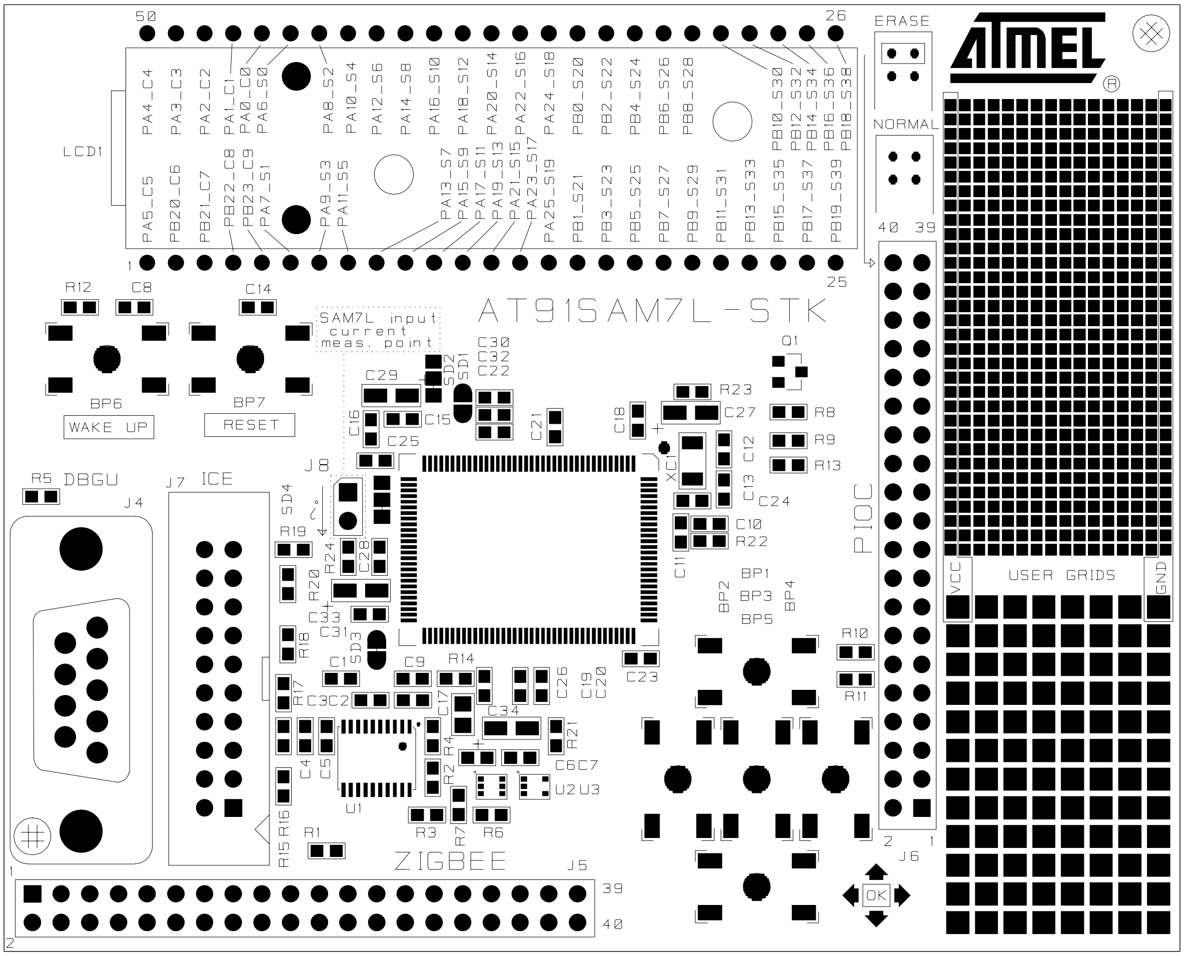
2.2 Requirements

In order to set up the AT91SAM7L-STK rev.A starter board, the following items are needed:

- The AT91SAM7L-STK rev.A starter board
- Two AAA batteries

2.3 Layout

Figure 2-1. AT91SAM7L-STK Rev. A Board Layout



2.4 Powering Up the Board

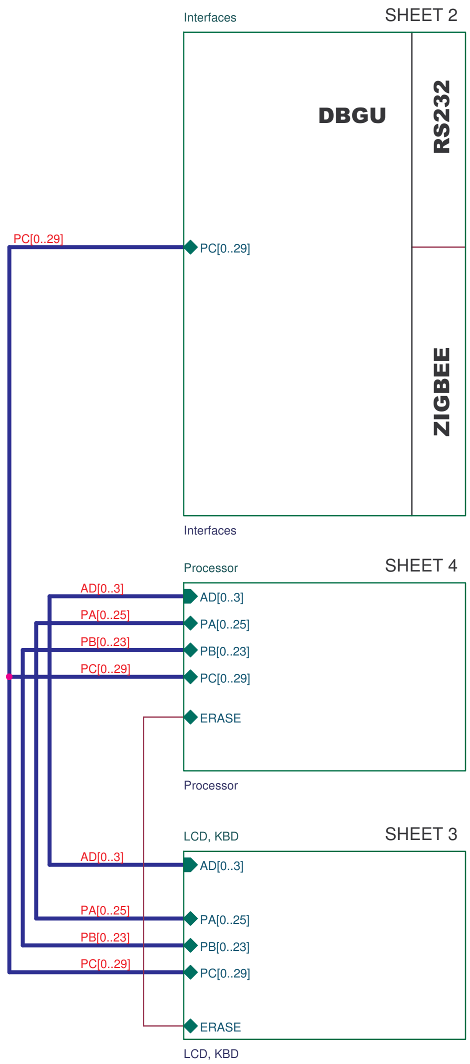
The AT91SAM7L-STK rev.A requires 3.0V (2.2V-3.6V) DC input. The power is supplied to the board via 2 AAA batteries or 3.0V VCC pads.

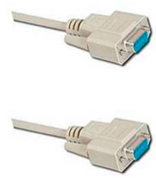
2.5 Getting Started

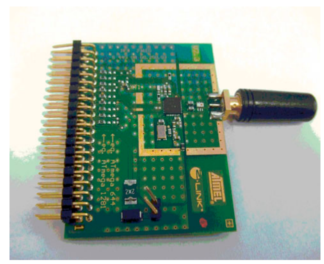
Please refer to the AT91SAM product pages on the Atmel web site, for the most up-to-date information on getting started with the AT91SAM7L-STK rev.A.

2.6 AT91SAM7L-STK Rev. A Block Diagram

Figure 2-2. AT91SAM7L-STK Block Diagram







Section 3

Board Description

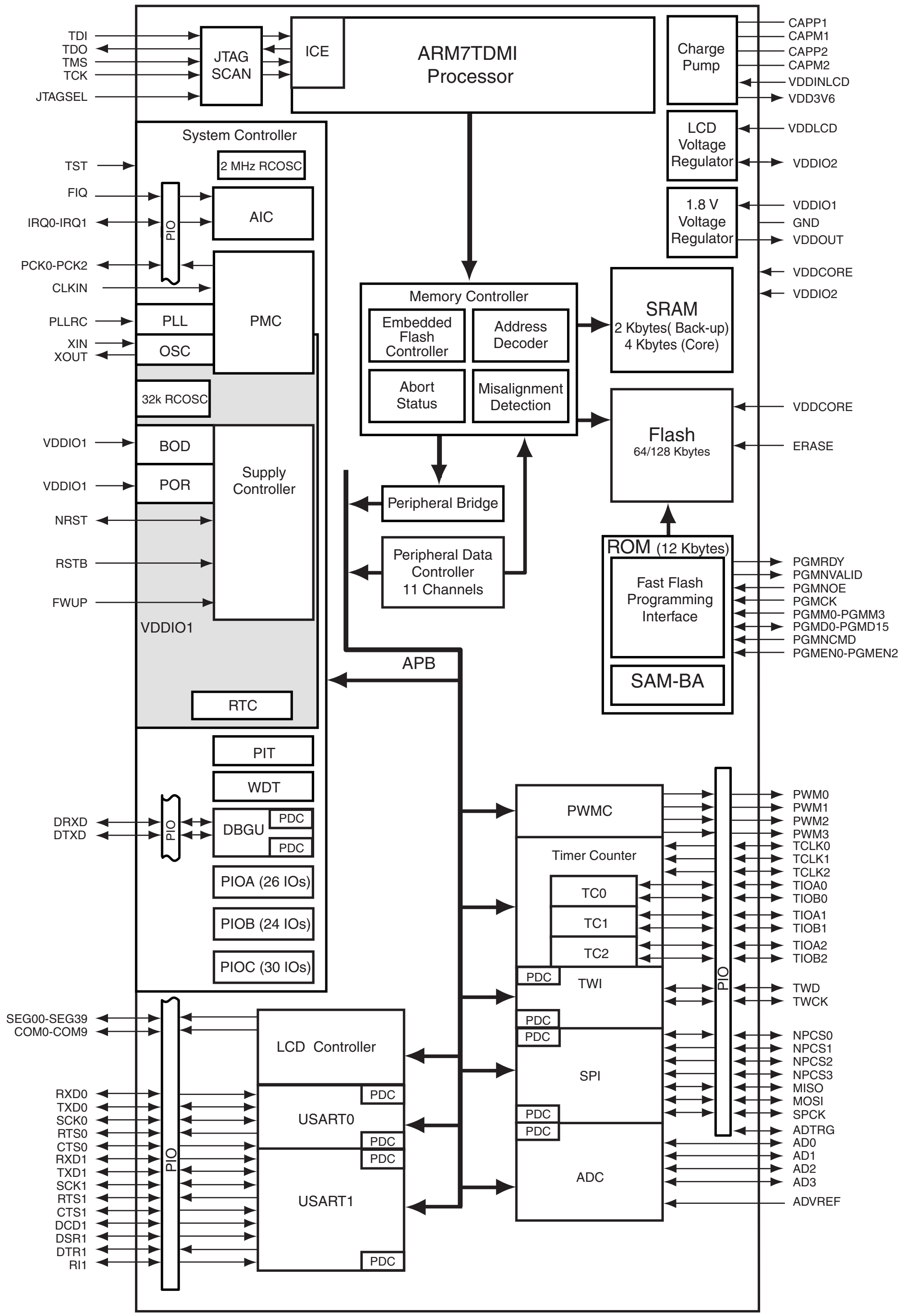
3.1 AT91SAM7L64/128 Microcontroller

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Internal High-speed Flash
  - 128 Kbytes (AT91SAM7L128), Organized in 512 Pages of 256 Bytes Single Plane
  - 64 Kbytes (AT91SAM7L64), Organized In 256 Pages of 256 Bytes Single Plane
  - Single Cycle Access at Up to 15 MHz in Worst Case Conditions
  - 128-bit Read Access
  - Page Programming Time: 4.6 ms, Including Page Auto Erase, Full Erase Time: 10 ms
  - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
  - Fast Flash Programming Interface for High Volume Production
- Enhanced Embedded Flash Controller (EEFC)
  - Interface of the Flash Block with the 32-bit Internal Bus
  - Increases Performance in ARM and Thumb Mode with 128-bit Wide Memory Interface
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
  - 6 kbytes
    - 2 Kbytes Directly on Main Supply that Can Be Used as Backup SRAM
    - 4 Kbytes in the Core
- Memory Controller (MC)
  - Enhanced Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
  - Based on Brownout Reset and Low-power Factory-calibrated Brownout Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power 32 kHz RC Oscillator, 32 kHz On-chip Oscillator, 2 MHz Fast RC Oscillator and one PLL
- Supply Controller (SUPC)
  - Minimizes Device Power Consumption
  - Manages the Different Supplies On Chip
  - Supports Multiple Wake-up Sources
- Power Management Controller (PMC)
  - Software Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
  - Three Programmable External Clock Signals
  - Handles Fast Start Up
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected

- **Debug Unit (DBGU)**
  - **Two-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention**
- **Periodic Interval Timer (PIT)**
  - **20-bit Programmable Counter plus 12-bit Interval Counter**
- **Windowed Watchdog (WDT)**
  - **12-bit Key-protected Programmable Counter**
  - **Provides Reset or Interrupt Signals to the System**
  - **Counter may be Stopped While the Processor is in Debug State or in Idle Mode**
- **Real-time Clock (RTC)**
  - **Two Hundred Year Calendar with Alarm**
  - **Runs Off the Internal RC or Crystal Oscillator**
- **Three Parallel Input/Output Controllers (PIOA, PIOB, PIOC)**
  - **Eighty Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os**
  - **Input Change Interrupt Capability on Each I/O Line**
  - **Individually Programmable Open-drain, Pull-up resistor and Synchronous Output**
- **Eleven Peripheral DMA Controller (PDC) Channels**
- **One Segmented LCD Controller**
  - **Display Capacity of Forty Segments and Ten Common Terminals**
  - **Software Selectable LCD Output Voltage (Contrast)**
- **Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
  - **Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation**
  - **Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support**
  - **Manchester Encoder/Decoder**
  - **Full Modem Line Support on USART1**
- **One Master/Slave Serial Peripheral Interface (SPI)**
  - **8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects**
- **One Three-channel 16-bit Timer/Counter (TC)**
  - **Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel**
  - **Double PWM Generation, Capture/Waveform Mode, Up/Down Capability**
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **One Two-wire Interface (TWI)**
  - **Master, Multi-Master and Slave Mode Support, All Atmel® Two-wire EEPROMs and I^{2}C compatible Devices Supported**
  - **General Call Supported in Slave Mode**
- **One 4-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os**
- **SAM-BA® Boot Assistant**
  - **Default Boot Program**
  - **Interface with SAM-BA Graphic User Interface**
  - **In Application Programming Function (IAP)**
- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **I/Os, including Four High-current Drive I/O lines, Up to 4 mA Each**
- **Power Supplies**
  - **Embedded 1.8V Regulator, Drawing up to 60 mA for the Core with Programmable Output Voltage**
  - **Single Supply 1.8V - 3.6V**
  - **Zero-power Power-on Reset and Brownout Detector, Fully Programmable**
- **Fully Static Operation: Up to 36 MHz at 85°C**
- **Available in a 128-lead LQFP Green and a 144-ball LFBGA Green Package**

3.2 AT91SAM7L64/128 Block Diagram

Figure 3-1. AT91SAM7L64/128 Block Diagram



3.3 Memory

- 6 Kbytes of Internal single-cycle access High-speed SRAM
- 64/128 Kbytes of Internal single-cycle access High-speed Flash

3.4 Clock Circuitry

- 32.768 KHz standard crystal for the oscillator

3.5 Reset Circuitry

- Internal reset controller with a bi-directional reset pin
- External reset push button

3.6 Shut Down controller

- Programmable shutdown and Wake-Up
- Wake-up push button.

3.7 Power Supply Circuitry

- For dynamic power consumption, the AT91SAM7L64/128 consumes a maximum of 30 mA on VCC at full speed 36MHz
- On board 2 AAA batteries or 3V DC input power pad directly supplied to VCC

3.8 User Interface

- Five user- input push buttons, four direction buttons and one ok button

3.9 Debug Interface

- 20-pin JTAG/ICE interface connector
- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket

3.10 Expansion Slot

- One ZIGBEE expansion connector for Atmel AT86RF230 adaptor
- All PIOC signals of the AT91SAM7L64/128 are routed to peripheral extension connector (J6). This allows the developer to add external hardware components or boards.

3.11 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PA0			Segment LCD PANEL	COM0	VDDIO2
PA1			Segment LCD PANEL	COM1	VDDIO2
PA2			Segment LCD PANEL	COM2	VDDIO2
PA3			Segment LCD PANEL	COM3	VDDIO2
PA4			Segment LCD PANEL	COM4	VDDIO2
PA5			Segment LCD PANEL	COM5	VDDIO2
PA6			Segment LCD PANEL	SEG0	VDDIO2
PA7			Segment LCD PANEL	SEG1	VDDIO2
PA8			Segment LCD PANEL	SEG2	VDDIO2
PA9			Segment LCD PANEL	SEG3	VDDIO2
PA10			Segment LCD PANEL	SEG4	VDDIO2
PA11			Segment LCD PANEL	SEG5	VDDIO2
PA12			Segment LCD PANEL	SEG6	VDDIO2
PA13			Segment LCD PANEL	SEG7	VDDIO2
PA14			Segment LCD PANEL	SEG8	VDDIO2
PA15			Segment LCD PANEL	SEG9	VDDIO2
PA16			Segment LCD PANEL	SEG10	VDDIO2
PA17			Segment LCD PANEL	SEG11	VDDIO2
PA18			Segment LCD PANEL	SEG12	VDDIO2
PA19			Segment LCD PANEL	SEG13	VDDIO2
PA20			Segment LCD PANEL	SEG14	VDDIO2
PA21			Segment LCD PANEL	SEG15	VDDIO2
PA22			Segment LCD PANEL	SEG16	VDDIO2
PA23			Segment LCD PANEL	SEG17	VDDIO2
PA24			Segment LCD PANEL	SEG18	VDDIO2
PA25			Segment LCD PANEL	SEG19	VDDIO2

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PB0			Segment LCD PANEL	SEG20	VDDIO2
PB1			Segment LCD PANEL	SEG21	VDDIO2
PB2			Segment LCD PANEL	SEG22	VDDIO2
PB3			Segment LCD PANEL	SEG23	VDDIO2
PB4			Segment LCD PANEL	SEG24	VDDIO2
PB5			Segment LCD PANEL	SEG25	VDDIO2
PB6			Segment LCD PANEL	SEG26	VDDIO2
PB7			Segment LCD PANEL	SEG27	VDDIO2
PB8			Segment LCD PANEL	SEG28	VDDIO2
PB9			Segment LCD PANEL	SEG29	VDDIO2
PB10			Segment LCD PANEL	SEG30	VDDIO2
PB11			Segment LCD PANEL	SEG31	VDDIO2
PB12	NPCS3		Segment LCD PANEL	SEG32	VDDIO2
PB13	NPCS2		Segment LCD PANEL	SEG33	VDDIO2
PB14	NPCS1		Segment LCD PANEL	SEG34	VDDIO2
PB15	RTS1		Segment LCD PANEL	SEG35	VDDIO2
PB16	RTS0		Segment LCD PANEL	SEG36	VDDIO2
PB17	DTR1		Segment LCD PANEL	SEG37	VDDIO2
PB18	PWM0		Segment LCD PANEL	SEG38	VDDIO2
PB19	PWM1		Segment LCD PANEL	SEG39	VDDIO2
PB20	PWM2		Segment LCD PANEL	COM6	VDDIO2
PB21	PWM3		Segment LCD PANEL	COM7	VDDIO2
PB22	NPCS1	PCK1	Segment LCD PANEL	COM8	VDDIO2
PB23	PCK0	NPCS3	Segment LCD PANEL	COM9	VDDIO2

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Peripheral Usage		Powered by
PC0	CTS1	PWM2	User's Input Buttons	OK	VDDIO1
PC1	DCD1	TIOA2	User's Input Buttons	UP	VDDIO1
PC2	DTR1	TIOB2	User's Input Buttons	RIGHT	VDDIO1
PC3	DSR1	TCLK1	User's Input Buttons	DOWN	VDDIO1
PC4	RI1	TCLK2	User's Input Buttons	LEFT	VDDIO1
PC5	IRQ1	NPCS2	ZIGBEE	IRQ1	VDDIO1
PC6	NPCS1	PCK2	ZIGBEE	NPCS1	VDDIO1
PC7	PWM0	TIOA0	MAX3318E	FORCEOFF	VDDIO1
PC8	PWM1	TIOB0	ZIGBEE	RSIN	VDDIO1
PC9	PWM2	SCK0	ZIGBEE	SLP_IR	VDDIO1
PC10	TWD	NPCS3			VDDIO1
PC11	TWCK	TCLK0			VDDIO1
PC12	RXD0	NPCS3	MAX3318E	FORCEON	VDDIO1
PC13	TXD0	PCK0	MAX3318E	INVALID	VDDIO1
PC14	RTS0	ADTRG	MAX3318E	READY	VDDIO1
PC15	CTS0	PWM3	VCC/VBAT MONITOR	ENABLE	VDDIO1
PC16	DRXD	NPCS1	MAX3318E	DRXD	VDDIO1
PC17	DTXD	NPCS2	MAX3318E	DTXD	VDDIO1
PC18	NPCS0	PWM0			VDDIO1
PC19	MISO	PWM1	ZIGBEE	MISO	VDDIO1
PC20	MOSI	PWM2	ZIGBEE	MOSI	VDDIO1
PC21	SPCK	PWM3	ZIGBEE	SPCK	VDDIO1
PC22	NPCS3	TIOA1			VDDIO1
PC23	PCK0	TIOB1			VDDIO1
PC24	RXD1	PCK1			VDDIO1
PC25	TXD1	PCK2			VDDIO1
PC26	RTS0	FIQ			VDDIO1
PC27	NPCS2	IRQ0			VDDIO1
PC28	SCK1	PWM0			VDDIO1
PC29	RTS1	PWM1			VDDIO1

Section 4

Configuration

4.1 Configuration Straps

Table 4-1 gives details of configuration straps on the AT91SAM7L-STK rev. A starter board and their default settings.

Table 4-1.

Designation	Default Setting	Feature
J6 pins 39-40	Opened	Closed for internal flash erase(1)
J8	Closed	VCC jumper(2)
SD1	Opened	Disables VDDIO2 to VDDLCD connection
SD2	2-3	Selects VCC or VDD3V6 to VDDLCD
SD3	Closed	Enables VDDOUT applying to VDDCORE
SD4	2-3	Selects VDDINLCD input
R20	IN	Enables the ICE NRST input
TP1	N.A	RX
TP2	N.A	TX
TP3	N.A	CLKIN
TP4	N.A	FWUP
TP5	N.A	ADREF
TP6	N.A	XOUT
TP7	N.A	NRSTB
TP8	N.A	VDDIO2
TP9	N.A	VDD3V6
TP10	N.A	VDDOUT

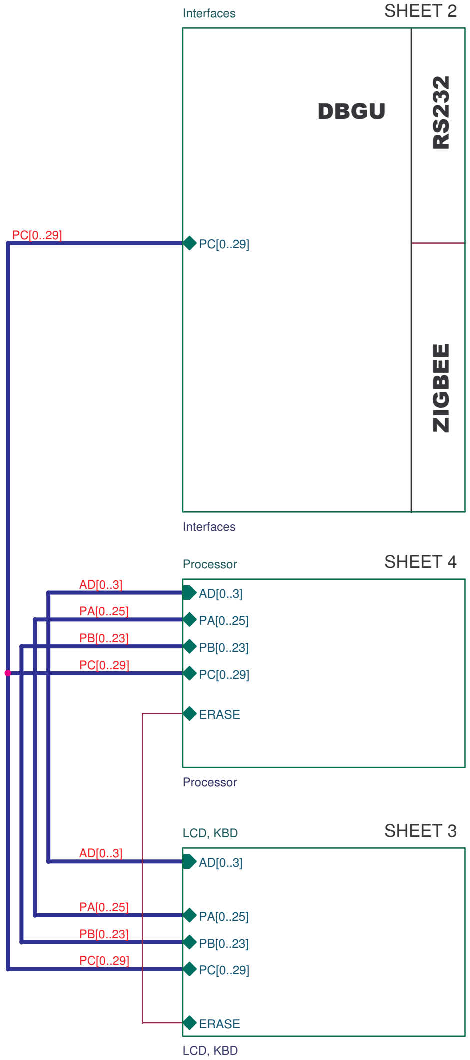
Notes: 1. This jumper is used to erase and reinitialize the internal flash content and some of the NVM bits.
2. This jumper is provided for power consumption measurement. By default, it is closed. To use this feature, the user has to open the strap and insert an ammeter.

Section 5

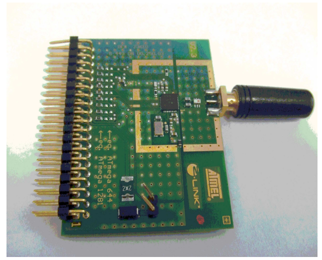
Schematics

This section contains the following schematics:

- Top Level
- Interfaces
- LCD, KBD
- Processor







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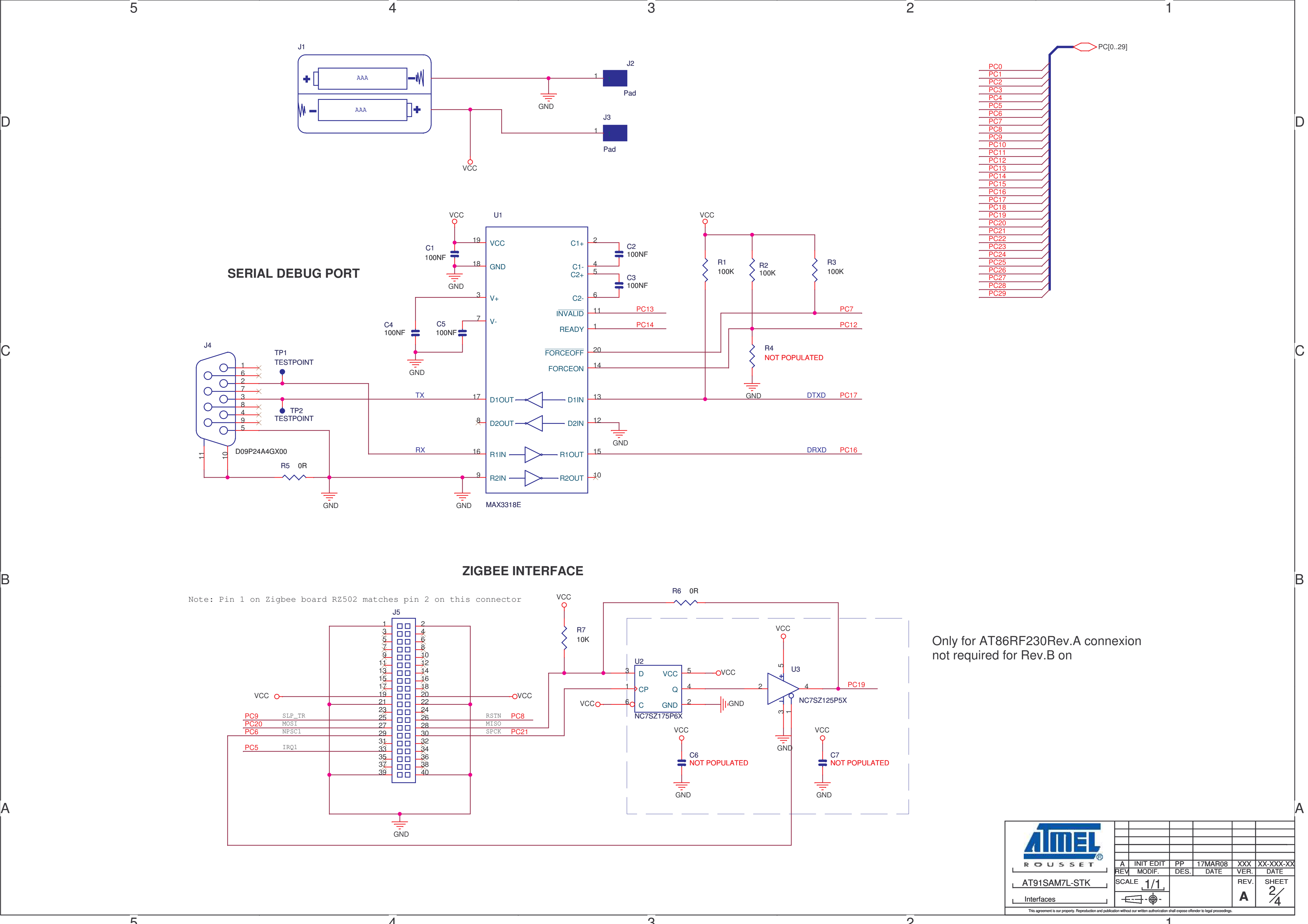
AT91SAM7L-STK

Top level

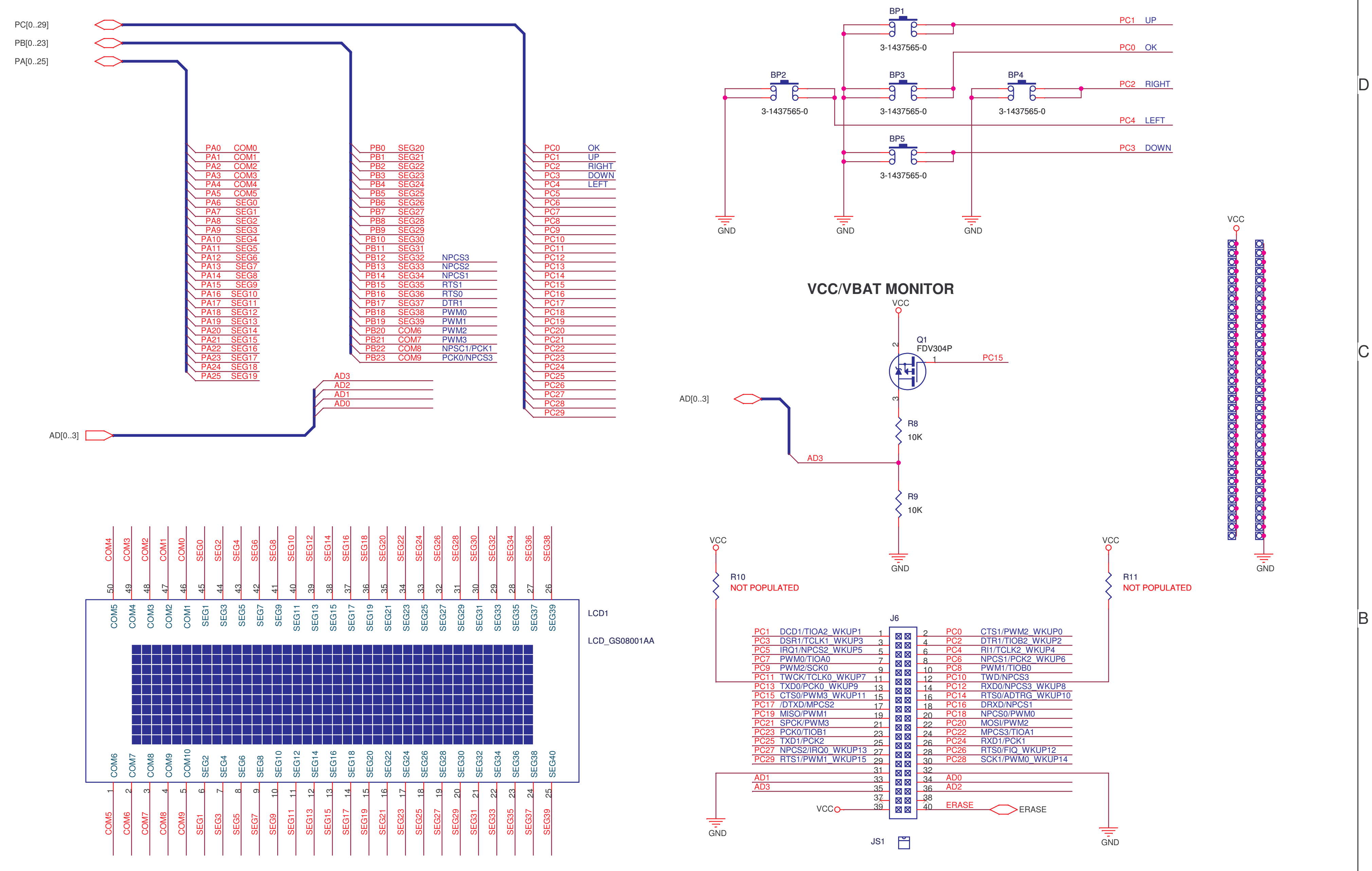
SCALE 1/1

REV. A

SHEET 1/4



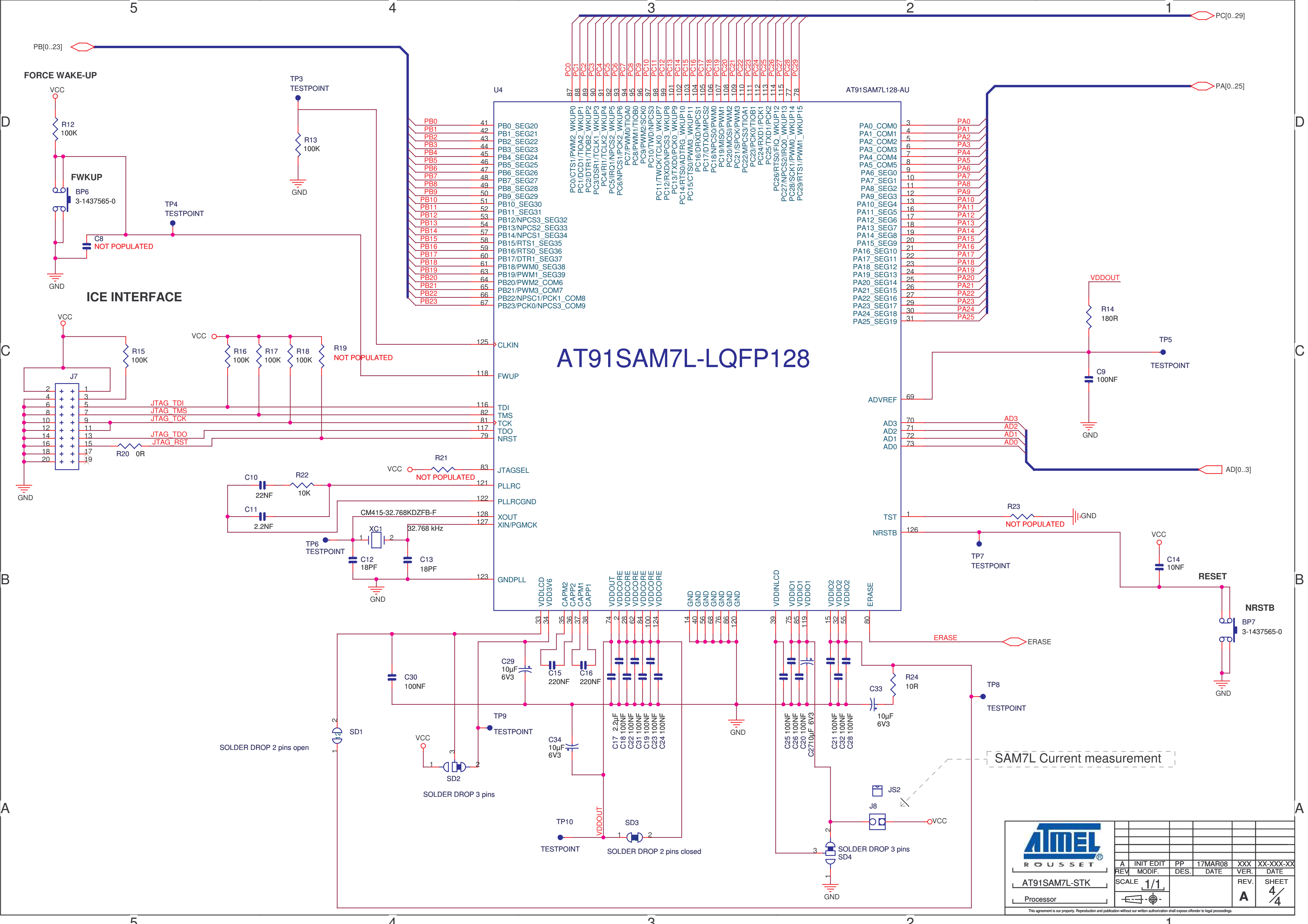
SERIAL DEBUG PORT
ZIGBEE INTERFACE
Note: Pin 1 on Zigbee board RZ502 matches pin 2 on this connector
Only for AT86RF230Rev.A connexion
not required for Rev.B on
J1
AAA
AAA
J2
Pad
J3
Pad
GND
VCC
PC[0..29]
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PC8
PC9
PC10
PC11
PC12
PC13
PC14
PC15
PC16
PC17
PC18
PC19
PC20
PC21
PC22
PC23
PC24
PC25
PC26
PC27
PC28
PC29
U1
MAX3318E
VCC
GND
V+
V-
C1+
C1-
C2+
C2-
INVALID
READY
FORCEOFF
FORCEON
D1OUT
D2OUT
R1IN
R2IN
D1IN
D2IN
R1OUT
R2OUT
C1 100NF
C2 100NF
C3 100NF
C4 100NF
C5 100NF
R1 100K
R2 100K
R3 100K
R4 NOT POPULATED
R5 0R
J4
D09P24A4GX00
TP1 TESTPOINT
TP2 TESTPOINT
TX
RX
DTXD
DRXD
J5
SLP_TR
MOSI
NPSC1
IRQ1
RSTN
MISO
SPCK
R6 0R
R7 10K
U2
NC7SZ175P6X
D
CP
C
Q
U3
NC7SZ125P5X
C6 NOT POPULATED
C7 NOT POPULATED
ROUSSET
AT91SAM7L-STK
Interfaces
A INIT EDIT PP 17MAR08 XXX XX-XXX-XX
REV MODIF. DES. DATE VER. DATE
SCALE 1/1
REV. A
SHEET 2/4
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SCALE 1/1				REV. A	SHEET 3/4

AT91SAM7L-STK

LCD, KBD


PB[0..23]
PC[0..29]
PA[0..25]
FORCE WAKE-UP
VCC
R12
100K
FWKUP
BP6
3-1437565-0
C8
NOT POPULATED
GND
TP3
TESTPOINT
R13
100K
TP4
TESTPOINT
ICE INTERFACE
U4
AT91SAM7L128-AU
AT91SAM7L-LQFP128
PB0_SEG20
PB1_SEG21
PB2_SEG22
PB3_SEG23
PB4_SEG24
PB5_SEG25
PB6_SEG26
PB7_SEG27
PB8_SEG28
PB9_SEG29
PB10_SEG30
PB11_SEG31
PB12/NPCS3_SEG32
PB13/NPCS2_SEG33
PB14/NPCS1_SEG34
PB15/RTS1_SEG35
PB16/RTS0_SEG36
PB17/DTR1_SEG37
PB18/PWM0_SEG38
PB19/PWM1_SEG39
PB20/PWM2_COM6
PB21/PWM3_COM7
PB22/NPSC1/PCK1_COM8
PB23/PCK0/NPCS3_COM9
PA0_COM0
PA1_COM1
PA2_COM2
PA3_COM3
PA4_COM4
PA5_COM5
PA6_SEG0
PA7_SEG1
PA8_SEG2
PA9_SEG3
PA10_SEG4
PA11_SEG5
PA12_SEG6
PA13_SEG7
PA14_SEG8
PA15_SEG9
PA16_SEG10
PA17_SEG11
PA18_SEG12
PA19_SEG13
PA20_SEG14
PA21_SEG15
PA22_SEG16
PA23_SEG17
PA24_SEG18
PA25_SEG19
PC0/CTS1/PWM2_WKUP0
PC1/DCD1/TIOA2_WKUP1
PC2/DTR1/TIOB2_WKUP2
PC3/DSR1/TCLK1_WKUP3
PC4/RI1/TCLK2_WKUP4
PC5/IRQ1/NPCS2_WKUP5
PC6/NPCS1/PCK2_WKUP6
PC7/PWM0/TIOA0
PC8/PWM1/TIOB0
PC9/PWM2/SCK0
PC10/TWD/NPCS3
PC11/TWCK/TCLK0_WKUP7
PC12/RXD0/NPCS3_WKUP8
PC13/TXD0/PCK0_WKUP9
PC14/RTS0/ADTRG_WKUP10
PC15/CTS0/PWM3_WKUP11
PC16/DRXD/NPCS1
PC17/DTXD/NPCS2
PC18/NPCS0/PWM0
PC19/MISO/PWM1
PC20/MOSI/PWM2
PC21/SPCK/PWM3
PC22/NPCS3/TIOA1
PC23/PCK0/TIOB1
PC24/RXD1/PCK1
PC25/TXD1/PCK2
PC26/RTS0/FIQ_WKUP12
PC27/NPCS2/IRQ0_WKUP13
PC28/SCK1/PWM0_WKUP14
PC29/RTS1/PWM1_WKUP15
CLKIN
FWUP
TDI
TMS
TCK
TDO
NRST
JTAGSEL
PLLRC
PLLRCGND
XOUT
XIN/PGMCK
GNDPLL
ADVREF
AD3
AD2
AD1
AD0
AD[0..3]
TST
NRSTB
VDDLCD
VDD3V6
CAPM2
CAPP2
CAPM1
CAPP1
VDDOUT
VDDCORE
GND
VDDINLCD
VDDIO1
VDDIO2
ERASE
J7
R15
100K
R16
100K
R17
100K
R18
100K
R19
NOT POPULATED
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_RST
R20 0R
R21
NOT POPULATED
C10
22NF
R22
10K
C11
2.2NF
CM415-32.768KDZFB-F
XC1
32.768 kHz
TP6
TESTPOINT
C12
18PF
C13
18PF
VDDOUT
R14
180R
TP5
TESTPOINT
C9
100NF
R23
NOT POPULATED
TP7
TESTPOINT
C14
10NF
RESET
NRSTB
BP7
3-1437565-0
ERASE
C30
100NF
C29
10µF
6V3
C15
220NF
C16
220NF
C17 2.2µF
C18 100NF
C22 100NF
C31 100NF
C19 100NF
C23 100NF
C24 100NF
C25 100NF
C26 100NF
C20 100NF
C27 10µF 6V3
C21 100NF
C32 100NF
C28 100NF
C33
10µF
6V3
R24
10R
TP8
TESTPOINT
TP9
TESTPOINT
SD1
SOLDER DROP 2 pins open
SD2
SOLDER DROP 3 pins
C34
10µF
6V3
TP10
TESTPOINT
SD3
SOLDER DROP 2 pins closed
SAM7L Current measurement
JS2
J8
SD4
SOLDER DROP 3 pins
ROUSSET
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AT91SAM7L-STK
Processor
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Section 6

Errata

6.1 Q1 Footprint Incorrect

Transistor Q1 is incorrectly connected. The schematic is right but the PCB connections of pins S and D are swapped => the protection diode is polarized forward (permanent current flow across the bridge) and the MOS is not operating properly (non accurate battery level measurement).

Problem Fix/Workaround

Remove Q1 in order to avoid the parasitic 150 µA battery drain. If battery measurement is really mandatory for some applications, Q1 has to be removed and soldered bottom up, taking care to apply the correct polarity. Additionally, a 100 KΩ pull-up resistor is needed across gate and source.

6.2 MAX3318 Control Pull-ups

The default configuration of the MAX3318 is ON. This leads to extra power consumption discharging the batteries when the AT91SAM7L128 enters OFF mode (or does not even drive PC7 and PC12 to put the MAX3318 in OFF mode).

Problem Fix/Workaround

Remove R1, R2 and R3 and add a 10M Ω pull-down resistor on PC7. This allows to Force OFF the MAX3318 when the AT91SAM7L128 enters OFF mode and to turn it on when the AT91SAM7L128 wakes up. The user can save power consumption by driving PC7 connected to the FORCEOFF pin of the MAX3318.

Section 7

Revision History

Doc Rev	Comments	Change Request Ref.
6409A	First issue.	

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